

HCMOS/TTL COMPATIBLE TRI-STATE VCXO IN CERAMIC LCC PACKAGE - VC53 Series

FEATURES

- RoHS Compliant (Pb-Free), Wide Frequency Pulling Range
- Very Low Phase Jitter with Fundamental Crystal Design

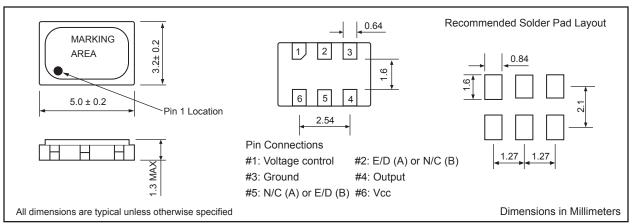
B = 3.3V

- Leadless Chip Carrier (LCC) Ultra Small Package with Industry de facto Standard Footprint
- Optional Enable/Disable Control at Either Pin #2 (VC53A) or Pin #5 (VC53B)

SPECIFICATIONS

Frequency Range	1 MHz to 108 MHz
Input Voltage (Vcc) Input Current Control Voltage (Vc) Storage Temperature Frequency Stability / APR (Min) Temperature Range Standard Stability / Pullability	A = +5 VDC \pm 5%; B = +3.3 VDC \pm 5% 15 mA Max for 3.3V and 20 mA Max for 5V +2.5V \pm 2.0V for 5.0V part; +1.65V \pm 1.5V for 3.3V part -55°C to 125°C A = \pm 50 / \pm 50 ppm; B = \pm 25 / \pm 50 ppm; C = \pm 50 / \pm 100 ppm; D = \pm 25 / \pm 75 ppm A = 0°C to 70°C; B = -40°C to 85°C; G = -10°C to 70°C BA = \pm 25 ppm / 0°C to 70°C, Absolute pull range (APR): \pm 50 ppm Minimum
Duty Cycle Output Load Logic "1" / Logic "0" Level Rise/Fall Time (Tr/Tf) Start-up time Phase Jitter (RMS, 1 Sigma) Modulation Bandwidth Linearity / Slope Input Impedance Setability at Fnom, 25°C Tristate Function Enable/Disable Time	1 = Tristate 60/40% symmetry; 3 = Tristate 55/45% symmetry HCMOS: drive up to 15 pF load; TTL: drive up to 10 TTL gates 0.9Vcc Minimum / 0.1Vcc Maximum 8 ns Maximum at 20% to 80% Vp-p 10 ms Maximum 1 ps Maximum for fj > 1kHz; 0.4 ps Typical for fj = 12KHz to 20MHz 12 kHz Minimum at -3 dB \pm 10% Maximum of best straight line fit / Positive 10 kOhms Minimum +2.5V \pm 0.5V for 5.0V part; +1.65V \pm 0.4V for 3.3V part Input (Pin 2 or 5) High (> 2.2V) or open: Output (Pin 4) active Input (Pin 2 or 5) Low (< 0.5V): Output disabled in high impedance 100 ns Maximum
Creating a Part Number Product Series A or B (see the Frequency	pelow)
	$B = \pm 257 \pm 50 \text{ ppm} \qquad \qquad X = \text{Outstomized temp range}$

OUTLINE DRAWING



C = ±50 / ±100 ppm D = ±25 / ±75 ppm