

## LV-PECL COMPATIBLE HIGH FREQUENCY VCXO IN LCC PACKAGE - VC75P1 Series

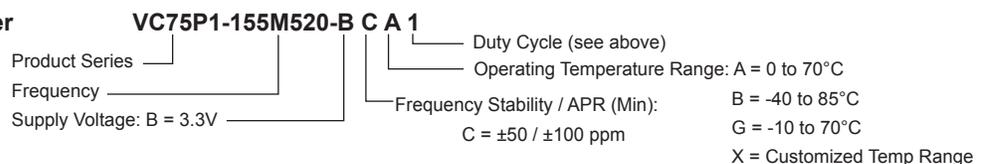
### FEATURES

- RoHS Compliant (Pb-Free), Wide Frequency Range
- Low Phase Jitter (4 ps at 155.52MHz) with New Generation PLL Design
- Leadless Chip Carrier Ultra Small Package with Industry de facto Standard Footprint
- Wide Frequency Pulling Range, APR =  $\pm 100$  ppm

### SPECIFICATIONS

<b>Frequency Range</b>	1 MHz to 800 MHz
<b>Input Voltage (Vcc)</b>	B = +3.3 VDC $\pm 5\%$
<b>Input Current</b>	100 mA Maximum
<b>Control Voltage (Vc)</b>	+1.65V $\pm 1.5V$
<b>Storage Temperature</b>	-55°C to 125°C
<b>Frequency Stability / APR (Min)</b>	C = $\pm 50$ / $\pm 100$ ppm
<b>Temperature Range</b>	A = 0°C to 70°C; B = -40°C to 85°C
<b>Standard Stability / Pullability</b>	CA = $\pm 50$ ppm / 0°C to 70°C, Absolute pull range (APR): $\pm 100$ ppm Minimum
<b>Duty Cycle</b>	1 = Tristate 60/40% symmetry; 3 = Tristate 55/45% symmetry
<b>Output Load</b>	50 Ohms to Vcc - 2.0V or Thevenin equivalent, Bias required
<b>Logic "1" / Logic "0" Level</b>	Vcc - 1.025V Minimum / Vcc - 1.620V Maximum
<b>Rise/Fall Time (Tr/Tf)</b>	1 ns Maximum at 20% to 80% Vp-p
<b>Start-up time</b>	5 ms Maximum
<b>Integrated Phase Jitter (RMS)</b>	4 ps Maximum for fj = 12KHz to 20MHz, at 155.520MHz
<b>Modulation Bandwidth</b>	12 kHz Minimum at -3 dB
<b>Linearity / Slope</b>	$\pm 20\%$ Maximum of best straight line fit / Positive
<b>Input Impedance</b>	50 kOhms Minimum, fm < 10KHz
<b>Setability at Fnom, 25°C</b>	+1.65V $\pm 0.4V$ for 3.3V part
<b>Tristate Function</b>	Input (Pin#2) High (2.2V Min) or open: Output (Pin#4, #5) active Input (Pin#2) Low (0.4V Max): Output disabled in high impedance
<b>Enable/Disable Time</b>	100 ns Maximum

### Creating a Part Number



### OUTLINE DRAWING

